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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,238	02/25/2002	Masanobu Hidehira	8039-1002	3861

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/081,238	HIDEHIRA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1, 3-9, and 11-15 are pending. Claims 2 and 10 have previously been cancelled. Claims 11-15 have previously been added.

Priority

Priority to Japanese Patent Application No. 2001-049492 (Feb. 23, 2001) is claimed.

Claim Objections

Claim 6 is objected to because of the following informalities:

As to claim 6, Applicant recites that the scanning line has a projecting portion overlapping at least one of said contact hole and said region where disclination occurs and shielding light. Such a limitation is confusing. The claim language is confusing because "at least one of" contradicts "and." Stating that the projecting portion overlaps at least one of the contact hole and disclination region means that the projecting portion overlaps either the contact hole or the disclination region but not both. Incorporation of "and" means that the projecting portion overlaps both the contact hole and the disclination region.

Furthermore, it is not clear as to whether the shielding light is another region or whether the projecting portion acts as a light shield.

For examination purposes, the Examiner presently interprets the limitation to mean that the scanning line has a projecting portion.

Appropriate correction is **required**.

Claim 8 is objected to because of the following informalities:

As to claim 8, Applicant recites that the projecting portion forms electrostatic capacitance between the wiring. Such a limitation is unclear. The claimed language is unclear because it is not known between what elements the electrostatic capacitance is formed. Because it is not clear as to what the projecting portion overlaps, it is also not clear as to between what elements the electrostatic capacitance is formed. The electrostatic capacitance is formed between the wiring and what else?

For examination purposes, the Examiner presently interprets the limitation to mean that the projecting portion forms an electrostatic capacitance.

Appropriate correction is **required**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,317,432 (to Ino).

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

As to claim 1, Shimada discloses a pair of substrates (Prior Art Figure 28, substrates 120 and 122), a liquid crystal sealed between said pair of substrates (Figure 28 LC 112), a plurality of gate signal lines and source signal lines crossing each other (Figures 16 A&B and 19), a switching element having one end of a current path connected to the corresponding data line and a control end connected to the corresponding scanning line (Figures 16 A&B and 19), a wiring connected to the other end of the current path of the switching element (Figures 16 A&B and Figure 19), an insulating layer being formed on said wiring and having a contact hole through which an end portion of said wiring is exposed (insulating film 136 of Figure 28), a pixel electrode being formed on said insulating layer and electrically connected to the end portion of said wiring through the contact hole (Figure 19, pixel 140); and an alignment film being formed on said pixel electrode and in contact with said liquid crystal (Figure 28, alignment film 150), wherein said contact hole is formed at a position overlapping a region where disclination occurs (Figure 16A and Figure 16B).

Please note that the pixel electrode is connected to the switching element through at least a wiring. The wirings of the switching element all have at least some type of shielding property.

Shimada does not appear to explicitly specify wherein said insulating layer is formed of a plurality of laminated insulating films, the insulating films have openings individually which form said contact hole in a tapered shape as a whole.

Ino teaches and discloses a liquid crystal display device with a capacitor and a thin film transistor in a trench for each pixel wherein with reference to Figures 24 and 31 by way of non-limiting examples, a first polysilicon layer (134) is formed on an insulating substrate (131) and a silicon oxide film (137) is formed on the first polysilicon layer (131) as a laminated structure (Figure 24, see also Figure 31 – insulating base 308, insulating film 309, resist 321 and opening 322). The films have therein a tapered shaped contact hole (at least opening 322 of Figure 31). Ino teaches that in the case that the substrate has a laminated structure of an insulating substrate and an insulating layer, an etching rate of the substrate as a whole can be improved (Abstract and entire patent).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ino (1) to improve upon the etching rate, (2) to form a tapered trench having a given depth in one step thus improving yield and also (3) to prevent disconnection (entire patent and Column 6, Lines 36-50).

As to claim 4, the wiring is made of a light shielding material and said contact hole and at least a part of the region where disclination occurs are shielded by said wiring (Shimada Column 7, Lines 61-63).

As to claim 5, the scanning lines and the data lines bounds a plurality of pixels each having said contact hole and said contact hole in the pixel is provided at a downstream in a

rubbing direction with respect to the switching element of other pixel adjacent to the pixel (Shimada Column 14, Lines 45-57).

As to claim 12, the boundary of the first and second regions of on source signal lines is covered with a light-shading film (Column 7, Lines 49-52).

Claims 3, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,317,432 (to Ino) and further in view of United States Patent 6,118,505 (to Nagata et al.).

As to claim 3, Shimada does not appear to explicitly specify that the insulating films include a passivation film formed on the switching element, a color layer formed on the passivation film and a flattening film formed on the passivation film and color layer where the contact hole includes openings formed in the passivation film, the color layer, and the flattening film respectively and the openings being formed in a tapered shape as a whole.

Nagata teaches and discloses a liquid crystal display device having a color organic film as an interlayer insulator (Title, entire patent). In regard to Figure 5B, by way of non-limiting example, a color organic insulating film (31) has a tapered wall shape to form a hole and an overcoat film (32) formed on the color organic film (31) also has a tapered wall shape to form a hole. The inner wall of each contact hole (33) is in a gentle taper shape so that the pixel electrode (15) is not disconnected (Column 14, Lines 23-29).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ino to prevent pixel electrode disconnection.

As to claims 9 and 11, Applicant's recited method steps would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in light of the devices as taught and disclosed by Shimada in view of Nagata.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,317,432 (to Ino) and further in view of United States Patent 5,831,707 (to Ota et al.).

As to claims 6 and 7, Shimada does not appear to explicitly specify that the scanning line has a projecting portion overlapping at least one of the contact hole and region where disclination occurs and shielding light, a black matrix has a wide portion overlapping a region in the pixel between said data line and the projecting portion and the projecting portion forms an electrostatic capacitance between the wiring.

Ota teaches and discloses an active matrix type liquid crystal display apparatus in which an insulating black matrix is formed at an interval between a pixel electrode and projection portion of a scan line (Column 22, Lines 29-33). The interval between the pixel electrode and projection portion is a necessary interval (Id.). The unnecessary intervals to which the reference refers, are those intervals other than the necessary interval between the pixel electrode and the scan line. Such a configuration improves contrast ratio (Id.).

Therefore it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ota for improved contrast ratio.

As to claim 8, the projection portion of the scan line forms an electrostatic capacitance.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,831,707 (to Ota et al.).

As to claim 13, Shimada discloses a pair of substrates (Prior Art Figure 28, substrates 120 and 122), a liquid crystal sealed between said pair of substrates (Figure 28 LC 112), a plurality of gate signal lines and source signal lines crossing each other (Figures 16 A&B and 19), a switching element having one end of a current path connected to the corresponding data line and a control end connected to the corresponding scanning line (Figures 16 A&B and 19), a wiring connected to the other end of the current path of the switching element (Figures 16 A&B and Figure 19), an insulating layer being formed on said wiring and having a contact hole through which an end portion of said wiring is exposed (insulating film 136 of Figure 28), a pixel electrode being formed on said insulating layer and electrically connected to the end portion of said wiring through the contact hole (Figure 19, pixel 140); and an alignment film being formed on said pixel electrode and in contact with said liquid crystal (Figure 28, alignment film 150), wherein said contact hole is formed at a position overlapping a region where disclination occurs (Figure 16A and Figure 16B). The wiring is made of a light shielding material and said contact hole and at least a part of the region where disclination occurs are shielded by said wiring (Shimada Column 7, Lines 61-63).

Please note that the pixel electrode is connected to the switching element through at least a wiring. The wirings of the switching element all have at least some type of shielding property.

Shimada does not appear to explicitly specify a black matrix overlapping data lines and that has a wide portion overlapping a region in the pixel between said data line and the projecting portion.

Ota teaches and discloses an active matrix type liquid crystal display apparatus in which an insulating black matrix is formed at an interval between a pixel electrode and projection portion of a scan line (Column 22, Lines 29-33). The interval between the pixel electrode and projection portion is a necessary interval (Id.). The unnecessary intervals to which the reference refers, are those intervals other than the necessary interval between the pixel electrode and the scan line. Such a configuration improves contrast ratio (Id.).

Therefore it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ota for improved contrast ratio.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,831,707 (to Ota et al.) and further in view of United States Patent 5,317,432 (to Ino).

As to claim 14, Shimada does not appear to explicitly specify wherein said insulating layer is formed of a plurality of laminated insulating films, the insulating films have openings individually which form said contact hole in a tapered shape as a whole.

Ino teaches and discloses a liquid crystal display device with a capacitor and a thin film transistor in a trench for each pixel wherein with reference to Figures 24 and 31 by way of non-limiting examples, a first polysilicon layer (134) is formed on an insulating substrate (131) and a silicon oxide film (137) is formed on the first polysilicon layer (131) as a laminated structure (Figure 24, see also Figure 31 – insulating base 308, insulating film 309, resist 321 and opening 322). The films have therein a tapered shaped contact hole (at least opening 322 of Figure 31). Ino teaches that in the case that the substrate has a laminated structure of an insulating substrate

and an insulating layer, an etching rate of the substrate as a whole can be improved (Abstract and entire patent).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ino (1) to improve upon the etching rate, (2) to form a tapered trench having a given depth in one step thus improving yield and also (3) to prevent disconnection (entire patent and Column 6, Lines 36-50).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,147,722 (to Shimada et al.) in view of United States Patent 5,831,707 (to Ota et al.) in view of United States Patent 5,317,432 (to Ino) and further in view of United States Patent 6,118,505 (to Nagata et al.).

As to claim 15, Shimada does not appear to explicitly specify that the insulating films include a passivation film formed on the switching element, a color layer formed on the passivation film and a flattening film formed on the passivation film and color layer where the contact hole includes openings formed in the passivation film, the color layer, and the flattening film respectively and the openings being formed in a tapered shape as a whole.

Nagata teaches and discloses a liquid crystal display device having a color organic film as an interlayer insulator (Title, entire patent). In regard to Figure 5B, by way of non-limiting example, a color organic insulating film (31) has a tapered wall shape to form a hole and an overcoat film (32) formed on the color organic film (31) also has a tapered wall shape to form a hole. The inner wall of each contact hole (33) is in a gentle taper shape so that the pixel electrode (15) is not disconnected (Column 14, Lines 23-29).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Shimada in view of Ino to prevent pixel electrode disconnection.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-9, and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

In view of the Appeal Brief filed on January 31, 2005, PROSECUTION IS HEREBY REOPENED.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER